Design and Analysis of On-Chip Symmetric Parallel-Plate Coupled-Line Balun for Silicon RF Integrated Circuits

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Abstract **In this paper, we present the design and analysis of an on-chip transformer balun for silicon RFIC. High-performance on-chip transformer baluns for low-noise amplifiers and power amplifiers on multi-layer radio-frequency integrated circuits are constructed. Single-end primary and differential secondary are constructed on different dielectric surface planes. The metal windings of the primary and secondary are in parallel to form coupled lines. Both the primary and the secondary are designed symmetrically for differential operation. Additional layer interfaces and vias are used to provide bridges to assure the geometric symmetry. Examples of designs with test results are discussed.**

I. Introduction

Transformers have been an essential component in radio-frequency (RF) electronic circuits for many decades. Recently, there have been many prior attempts to integrate transformer and/or baluns on-chip in RFIC [1-5]. Prior work on on-chip transformers is best summarized in Reference [4]. Various transformer layouts including parallel winding, inter-wound winding, overlay winding, and concentric spiral winding were discussed. Several factors limit the application of on-chip transformers in RFIC. First, the magnetic core that is commonly used in electric circuits to confine magnetic flux is not applicable. As a result, the flux leakage and capacitive coupling degrade the transformer performance. Second, the series resistance associated with the metal windings is often significant due to the fact that the metal thickness is usually much less than its skin depth in present silicon IC process. The resulting current consumption and power loss at the transformer are usually much higher than what is desirable. Recently, we proposed a transformer/balun structure [6] in the form of spiral multi-layer windings for both primary and secondary with smaller size as compared with other similar on-chip balun. For balun application, the existing structures are not symmetric, resulting in the degradation of differential signals. The requirements of the on-chip transformer baluns for LNA and PA are quite demanding. For practical purposes, the on-chip transformer balun must be small and compatible with the size of other on-chip inductors. For an LNA, the balun needs to provide enough voltage gain (typically 10-15 dB) with low noise figure (NF). NF is directly related to the quality factor (Q) of the transformer balun. Usually the higher Q is, the lower the noise figure would be. In silicon RFIC, the Q is usually low and limited by the metal thickness and metal resistivity. For PA, the balun track width needs to be wide to support large current density. The Q also needs to be high to have high efficiency and high PA linearity. It also requires current amplification to provide large current swing at antenna output. The baluns for both LNA and PA also need to be inductive enough such that only on-chip MIS capacitors would be needed for tuning to match with antenna impedance. Hence, it is necessary that the transformer baluns are symmetric such that LNA and PA would see the same impedance at the two differential ports.

In this paper, we propose a new on-chip transformer structure utilizing the characteristics of parallel-plate line coupling [7]. An example of a generic structure with 3:3 turn ratios is shown in Figure 1. A unique feature is that symmetric metal windings (or symmetric inductors) are used in both primary and secondary, each resided on different metal layers. The primary and secondary can be any number of turns (limited by the capacitance and area) and are both symmetric. The designs of the proposed structures that meet the technical requirements will be discussed with confirmation from the measured data.

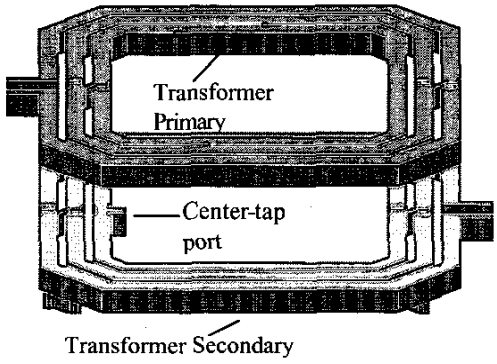

Figure 1. Perspective view of a parallel-plate coupled-line transformer baluns on multi-layer radio-frequency integrated circuits.

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II. Design, Simulation, and Models

As was shown in Figure 1, the primary and secondary windings occupy a total of two metal layers. However, as was pointed out in [4], in order to have symmetric metal windings, additional bridge layers are needed for multi-turn interconnects. Figure 2 shows the underside view of the same structure in Figure 1 to demonstrate the bridge connection. Part of the crossover windings need to go through the bridge layer with vias to maintain geometric symmetry and close vicinity of ports.

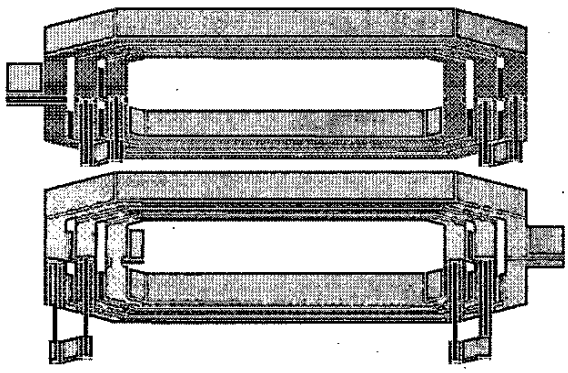

Figure 2: An underside view of the same structure shown in Figure 1 to detail the bridge connections for the primary and secondary.

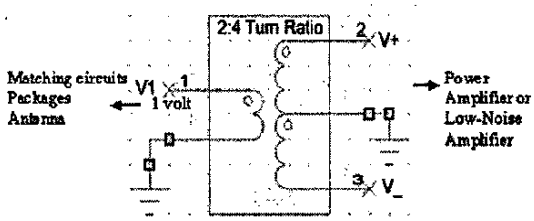

Figure 3. Three-port transformer balun circuit model.

Numerical simulations and experiments are carried out to demonstrate the feasibility of the proposed transformer structure. On-chip transformer baluns are built on a four metal-layer thin-film silicon semiconductor structure. As an example, two-turn windings are placed at both the first and the second metal layers shunted together through vias to form the primary. Four-turn metal windings are placed at the fourth metal layer with the third metal layer as the bridge layer resembling the structure in Figure 1. In principle, the primary and secondary winding should be separately as far as possible (vertically) to reduce the capacitance. The first two metal layers are shunted together to increase the Q of the primary (reducing series resistance). The top metal layer thickness is 0.92μm and the rest metal layer thickness is 0.64μm. All the metal layers are made of aluminum. The corresponding balun circuit model is shown in Figure 3. It is a three-terminal device, where port 1 is the single-end port and ports 2 and 3 are differential ports. The differential-port signals (2 and 3) are ideally the same in magnitude but 180 degrees phase difference. The simulation is based on the IE3D three-dimensional full-wave simulator. In simulation, the transformer balun is modeled as a five-port circuit. In post processing, one primary port and the center-tap port are grounded as demonstrated in Figure 3. The three-port circuit parameters are measured using a network analyzer where only two-port connection is available. Complete three-port Z-matrix is obtained by performing the two-port measurement three times and in each time, one of the ports is open-circuited in alternation. The input voltage is normalized to 1 and the output voltages (at the secondary) are the open-circuit voltages. In practice, either LNA or PA is high-impedance (capacitive) and the open-circuit voltage is close to the actual value.

Table I. Comparison of simulated and measured results to show the validity of the concept of invention

Simulation Tool: IE3D three-dimensional full-wave simulator
Open-Circuit Secondary for Phase and Amplitude Balance Check

F=2.43 GHz	Z11	Z12	Z13	Z22	Z23	Z33
Simulation	9.3+j 27.3	3.3+j 24.1	-3.7-j24.4	10.7+j29.6	-2.6-j23.5	11.3+j30.4
Measurement	9.2+j 28.0	2.9+j 24.4	-3.0-j24.9	9.5+j 31.3	-1.9-j23.0	9.8+j 31.5

Frequency (GHz)	Simulated |V+|	Measured |V+|	Simulated |V_|	Measured |V_|	Simulated Phase Diff of V+ and V-	Measured Phase Diff of V+ and V-
2.40	0.8538	0.8489	0.8429	0.8472	180.71	180.41
2.43	0.8549	0.8525	0.8438	0.8517	180.72	180.70
2.46	0.8559	0.8549	0.847	0.8542	180.73	180.23

The outer dimension of the balun is 275μm by 275μm and the track width is designed wide enough to handle high current density for PA. The resistive loss at the balun is not a major issue for PA application due to the fact that balun is also part of the impedance match circuit. The balun efficiency is about 45%, while conjugate matching introduces 50% matching loss.

The comparison between simulated and test results are given in Table I. It shows the phase error less than 1 degree and amplitude error less than 0.1%. The balun is

designed for the use around 2.43 GHz. Another interesting observation is the voltage ratio. For a perfect transformer with 2 to 4 turn ratios, the differential voltage should be 1 volt with 1 volt primary. The measurement shows that this voltage is about 0.85 and it is also the coupling coefficient. This value is fairly high as compared to other on-chip transformer baluns [7].

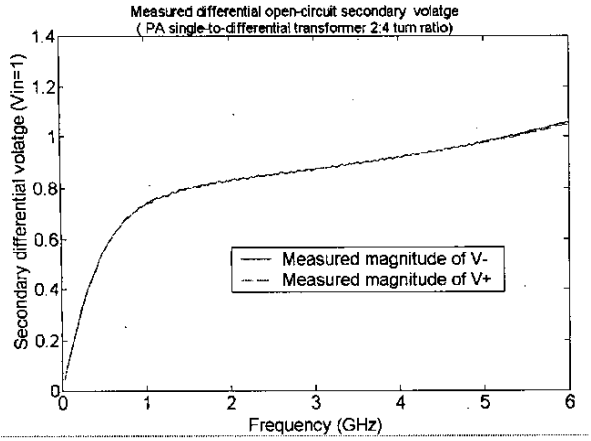

Figure 4. Frequency response of transformer voltage ratio of the designed on-chip balun.

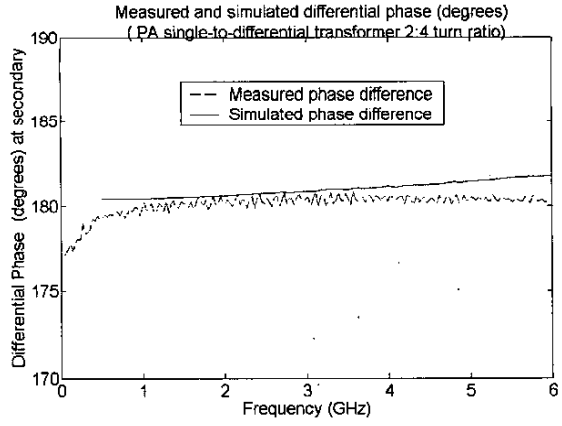

Figure 5. Frequency response of differential phase output at the secondary.

Frequency response of voltage transformation from primary to secondary is shown in Figures 4 and 5 for voltage ratio and for differential phase, respectively. Excellent balun characteristics over a broad frequency range are observed.

The distinctive feature of this structure is that primary and secondary are geometrically parallel to each other. Either primary or secondary can be on top of the other. Also, either one can have additional layer of identical winding in shunt to reduce the resistive loss.

III. Design and Layout Considerations

Figure 6 shows the top view of a three-turn primary as an example, which by itself is a differential inductor without a ground tap. The multi-turn spiral-type primary is made in an octagon shape to minimize the ohmic loss. In balun, terminal 1 is the signal port, terminal 2 is ground and the primary is like a single-end inductor. In order to keep ports 1 and 2 close and symmetric, crossover interconnects are needed. As shown in Figure 6, metal strips are connected through a bridge on a lower layer with vias. Figure 7 shows an example of a nine-turn secondary, which by itself can be used as a symmetric differential inductor. In order to produce differential signals at terminal 1 and terminal 2, the geometric center would need to be grounded. The center is at the inner side of the winding and has to be brought out to ground physically. A rectangular bridge with vias is used for connection to the center point. The center-tap ground is at the terminal 3.

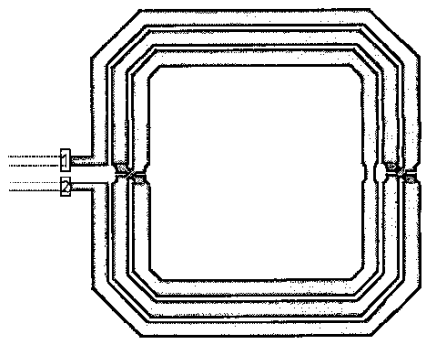

Figure 6. The top view of a three-turn primary of the transformer balun.

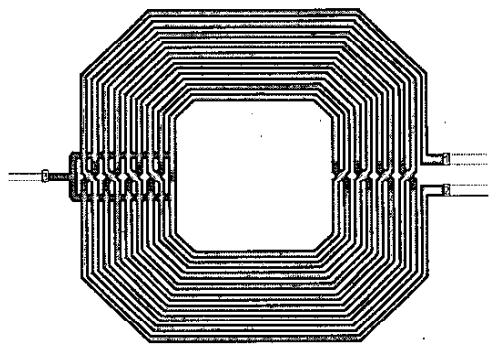

Figure 7. The top view of a nine-turn secondary of the transformer balun.

For balun, the differential terminals at secondary are connected to two separate circuits and it is useful that the impedance looking back into each terminal is the same. A balun with geometric symmetry would meet this goal. The metal strips in the primary and secondary form parallel-plate coupled lines. The coupling of the signal from primary to secondary is due to both magnetic flux linkage through the internal area and the capacitive coupling of parallel-plate coupled (top and bottom) lines. This vertical coupling provides good coupling coefficient (85% coupling efficiency is obtained). In silicon RFIC structure, the upper metal layer is usually thicker than the lower ones and therefore, with less ohmic loss. For the design consideration, it is possible that the secondary is on the upper metal layer and primary on the lower layer. It is also possible to use two identically metal layers in shunt to reduce ohmic loss as is the case of the design here.

The design of an on-chip transformer balun depends on specific applications. For example, the balun for LNA is to generate differential signals to the LNA from signal at antenna in a receiver mode. The load looking into LNA determines the overall size and turn ratio so that the on-chip impedance matching is applicable, the gain is maximized, and the noise figure is at an acceptable level. Note that for the balun under consideration, the primary and secondary currents are in opposite directions. The inductance of the primary, not the resistance is reduced or sometimes dictated by the induced flux in the secondary.

The secondary loading will usually reduce the primary Q and inductance while increases the capacitance. The reduction of the balun size will help increase the inductance. Since high impedance load at the differential ports is usually the case, Q of the primary dictates the power loss and noise figure at the balun. In order to obtain a differential output, a center-tap ground is placed roughly midway through the secondary windings. The precise location can only be determined by several trial and errors in simulation.

IV. Conclusions

This paper described a compact on-chip RFIC transformer balun. Each multi-turn primary and secondary is constructed on a separate metal layer within a multi-layer dielectric substrate. The metal windings of the primary and secondary, both are symmetric to their geometric center, are in parallel to form a parallel-plate microstrip lines. The proposed balun structure has advantage of strong coupling coefficient (85%), excellent symmetry, and small size. It was demonstrated with both simulation and experiment that the described balun structure provides excellent differential amplitude and phase balance. The proposed balun can be easily integrated with either LNA or PA on the chip-front end and can be also used for impedance matching to the antennas.

III. References

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